54SX Family FPGAs

Features

High Performance

- 320 MHz Internal Performance
- 4.0 ns Clock-to-Out (Pin-to-Pin)
- 0.6 ns Input Set-Up
- 0.25 ns Clock Skew

High Density

- 8,000 to 32,000 Available Logic Gates
- 246 User-Programmable I/O
- 1,080 Flip-Flops

Easy Logic Integration

- ASIC Design Methodology Support Using Synthesis Tools for Performance-Intensive Designs
- 100% Resource Utilization with 100% Pin Locking
- 3.3V Operation with 5.0V Input Tolerance
- Low Power Consumption
- Deterministic, User-Controllable Timing
- Unique, In-System Diagnostic and Debug Facility with Silicon Explorer
- JTAG Boundary Scan Testing in Compliance with IEEE Standard 1149.1
- Actel Designer Series Design Tools, Supported by Cadence, Exemplar, IST, Mentor Graphics, Model Tech, Synopsys, Synplicity, and Viewlogic Design Entry and Simulation Tools
- Permanently Programmed for Instantaneous Operation on Power-Up
- Secure Programming Technology Prevents Reverse Engineering and Design Theft

General Description

The New SX Family of FPGAs

Actel's SX Family of FPGAs features a revolutionary new sea-of-modules architecture that delivers next-generation device performance and integration levels not currently achieved by any other FPGA architecture. SX devices greatly simplify design time, enable dramatic reductions in design costs and power consumption, and further speed time-to-market for performance-intensive applications.

SX Product Profile

	A54SX08	A54SX16	A54SX32
Gates	8,000	16,000	32,000
Logic Modules	768	1,452	2,880
Flip-Flop Modules	256	528	1,080
Combinatorial Modules	512	924	1,800
User I/Os (Maximum)	129	177	246
JTAG	Yes	Yes	Yes
Clock-to-Out (Pin-to-Pin)	4.0 ns	4.4 ns	TBD
Input Set-Up (External)	0.6 ns	0.6 ns	TBD
Packages (by pin count)			
PQFP	208	208	208
PLCC	84	84	84
VQFP	100	100	—
TQFP	176	176	176
CQFP	—	208, 256	208, 256
EBGA	329	329	329
PBGA	—	—	313

Fast and Flexible New Architecture

Actel's SX architecture features two types of logic modules, the combinatorial cell (C-cell) and the register cell (R-cell), each optimized for fast and efficient mapping of synthesized logic functions. Optimal use of the silicon is made by locating the routing and interconnect resources in the metal layers above the logic modules, enabling the entire floor of the device to be spanned with an uninterrupted grid of fine-grained, synthesis-friendly logic modules (or "sea-of-modules") which reduces the distance signals have to travel between logic modules.

To minimize signal propagation delay, SX devices employ both local and general routing resources. The high-speed local routing resources (DirectConnect and FastConnect) enable very fast local signal propagation that is optimal for fast counters, state machines, and datapath logic. The general system of segmented routing tracks allows any logic module in the array to be connected to any other logic or I/O module. Within this system, propagation delay is minimized by limiting the number of antifuse interconnect elements to five (typically 90% of connections use only two antifuses). The unique local and general routing structure featured in SX devices gives fast and predictable performance, allows 100% pin-locking with full logic utilization, enables concurrent PCB development, reduces design time, and allows designers to achieve performance goals with a minimum of effort.

Further complementing the SX's flexible routing structure, a hard-wired, constantly-loaded clock network has been tuned to provide fast clock propagation with minimal clock skew. Additionally, the high performance of the internal logic has eliminated the need to embed latches or flip-flops in the I/O cells to achieve fast clock-to-out or fast input set-up times. SX devices have easy-to-use I/O cells which do not require HDL instantiation, facilitating design re-use and reducing design and debugging time.

Ordering Information

A54SX16 – 2 PQ 208

Application (Temperature Range)
- Blank = Commercial (0 to +70°C)
- I = Industrial (–40 to +85°C)
- M = Military (–55 to +125°C)
- B = MIL-STD-883

Package Lead Count

Package Type
- BG = Ball Grid Array
- CQ = Ceramic Quad Flat Pack
- PL = Plastic Leaded Chip Carrier
- PQ = Plastic Quad Flat Pack
- TQ = Thin (1.4 mm) Quad Flat Pack
- VQ = Very Thin (1.0 mm) Quad Flat Pack

Speed Grade
- Blank = Standard Speed
- –1 = Approximately 15% Faster than Standard
- –2 = Approximately 25% Faster than Standard

Part Number
- A54SX08 = 8,000 Gates
- A54SX16 = 16,000 Gates
- A54SX32 = 32,000 Gates

Product Plan

	Speed Grade			Application			
	Std	–1*	–2*	C	I	M	B
A54SX08 Device							
84-Pin Plastic Leaded Chip Carrier (PLCC)	P	P	P	P	P	—	—
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	P	P	P	P	P	—	—
176-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	—	—
208-Pin Plastic Quad Flat Pack (PQFP)	P	P	P	P	P	—	—
329-Pin Enhanced Ball Grid Array (EBGA)	P	P	P	P	P	—	—
A54SX16 Device							
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	P	P	—	—
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	P	P	—	—
176-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	—	—
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	P	P	—	—
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	—	P	—	P	P
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	—	P	—	P	P
329-Pin Enhanced Ball Grid Array (EBGA)	P	P	P	P	P	—	—
A54SX32 Device							
84-Pin Plastic Leaded Chip Carrier (PLCC)	P	P	P	P	P	—	—
176-Pin Thin Quad Flat Pack (TQFP)	P	P	P	P	P	—	—
208-Pin Plastic Quad Flat Pack (PQFP)	P	P	P	P	P	—	—
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	—	P	—	P	P
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	—	P	—	P	P
313-Pin Enhanced Ball Grid Array (EBGA)	P	P	P	P	P	—	—
329-Pin Enhanced Ball Grid Array (EBGA)	P	P	P	P	P	—	—

Consult your local Actel sales representative for product availability.

Applications: *C = Commercial* *I = Industrial* *M = Military* *B = MIL-STD-883*

Availability: ✔ = *Available* *P = Planned* — = *Not Planned*

** Speed Grade:* *–1 = Approx. 15% Faster than Standard* *–2 = Approx. 25% Faster than Standard*

Device Resources

Device	User I/Os					
	PLCC 84-Pin	VQFP 100-Pin	PQFP 208-Pin	TQFP 176-Pin	PBGA 313-Pin	EBGA 313-Pin
A54SX08	66	78	129	129	—	129
A54SX16	66	78	172	144	—	177
A54SX32	66	—	172	144	246	246

Package Definitions *(Consult your local Actel sales representative for product availability.)*

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array, EBGA = Enhanced Ball Grid Array

Pin Description

CLKA Clock A (Input)

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

CLKB Clock B (Input)

TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

TCK Test Clock (Input)

Test clock input for diagnostic probe and device programming. In flexible mode (refer to the JTAG pins functionality table), TCK becomes active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the "logic reset" state.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock (Input)

TTL clock input for sequential modules. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output (Input, Output)

The I/O pin functions as an input, output, three-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are tri-stated by the Designer Series software.

TMS Test Mode Select (Input)

The TMS pin controls the use of JTAG pins (TCK, TDI, TDO). In flexible mode (refer to the JTAG pins functionality table), when the TMS pin is set LOW, the TCK, TDI, and TDO pins are JTAG pins. Once the JTAG pins are in JTAG mode they will remain in JTAG mode until the internal JTAG state machine reaches the "logic reset" state. At this point the JTAG pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated JTAG mode, TMS functions as specified in the IEEE 499.1 JTAG Specifications.

NC No Connection

This pin is not connected to circuitry within the device.

PRA ActionProbe A (Output)

The ActionProbe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the ActionProbe B pin to allow real-time diagnostic output of any signal path within the device. The ActionProbe A pin can be used as a user-defined I/O when debugging has been completed.

PRB ActionProbe B (Output)

The ActionProbe B pin is used to output data from any node within the device. This diagnostic pin can be used in conjunction with the ActionProbe A pin to allow real-time diagnostic output of any signal path within the device. The ActionProbe B pin can be used as a user-defined I/O when debugging has been completed.

TDI Test Data Input (Input)

Serial input for JTAG and diagnostic probe. In flexible mode, (refer to the JTAG pins functionality table), TDI is active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the "logic reset" state.

TDO Test Data Output (output)

Serial output for JTAG. In flexible mode. (Refer to the JTAG pins functionality table), TDO is active when the TMS pin is set LOW. This pin functions as an I/O when the JTAG state machine reaches the "logic reset" state.

V_{CCI} 3.3V Supply Voltage

3.3V supply voltage for I/Os.

V_{CCA} 3.3V Supply Voltage

3.3V supply voltage for Array.

V_{CCR} 5V Supply Voltage

5V supply voltage for input tolerance (required for internal biasing).

SX JTAG Pins Functionality Table

SX devices offer superior diagnostic and testing capabilities by providing JTAG and probing capabilities. These functions are controlled through the special JTAG pins in conjunction with the program fuse. The functionality of each pin is described in Table 1 below.

Table 1 • JTAG

Program Fuse Blown (Dedicated JTAG Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated JTAG pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10K ohm on TMS

In the dedicated JTAG mode, TCK, TDI and TDO are dedicated JTAG pins and cannot be used as regular I/Os. In flexible mode, TMS should be set HIGH through a pull-up resistor of 10K ohm. TMS can be pulled LOW to initiate the JTAG sequence.

The program fuse determines whether the device is in dedicated or flexible mode. The default (fuse not blown) is flexible mode.

SX Family Architecture

The SX Family architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of applications.

Programmable Interconnect Element

Actel's new SX Family provides much more efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (see Figure 1). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the M2 and M3 layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements gives the SX Family abundant routing resources and provides excellent protection against design pirating. Reverse engineering is virtually impossible as it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and there is no configuration bitstream to intercept.

Additionally, the interconnect (i.e., the antifuses and metal tracks) have lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry.

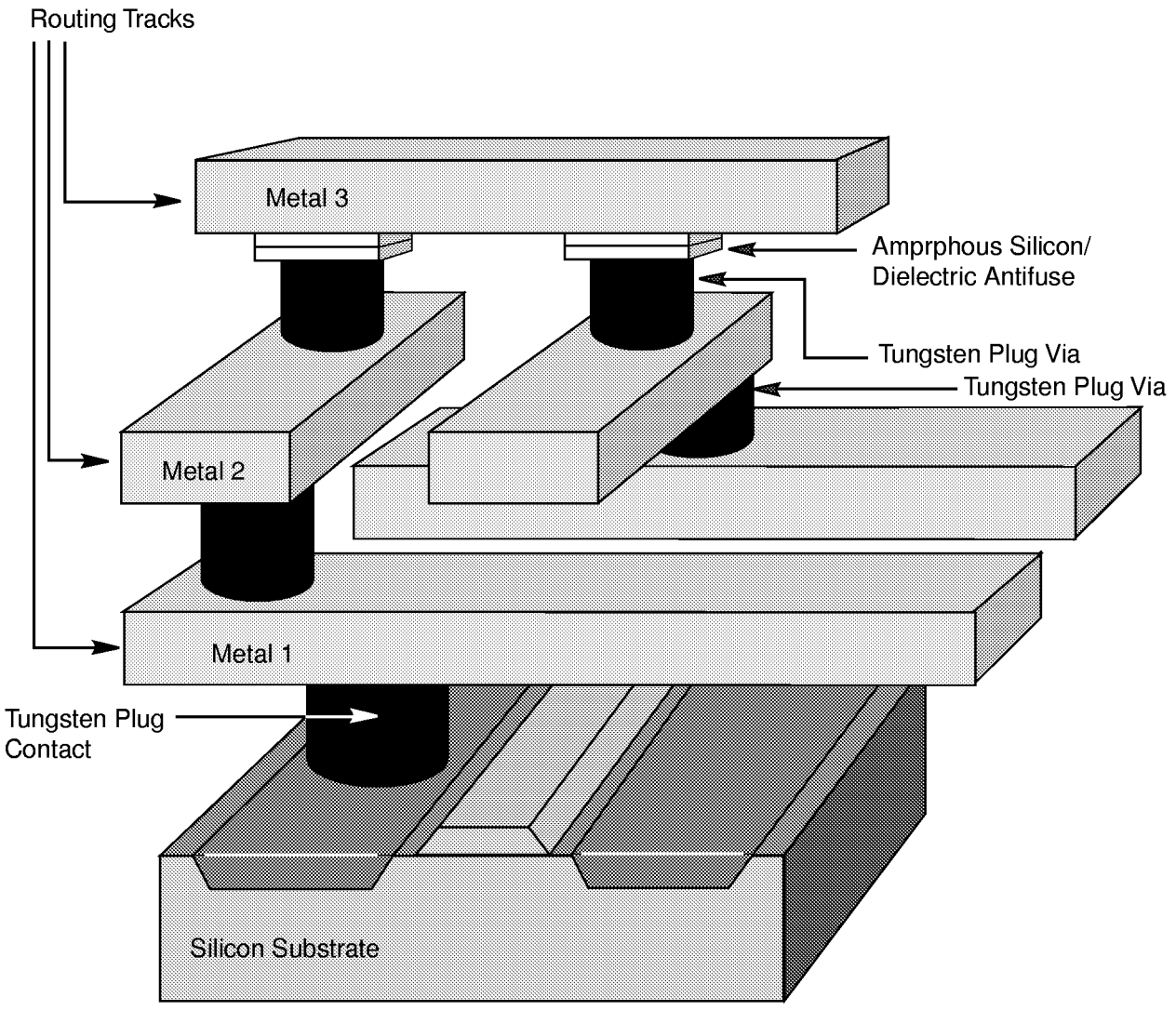


Figure 1 • *SX Family Interconnect Elements*

Logic Module Design

The SX Family architecture has been called a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing (see Figure 2). Actel provides two types of logic modules, the R-cell and the C-cell.

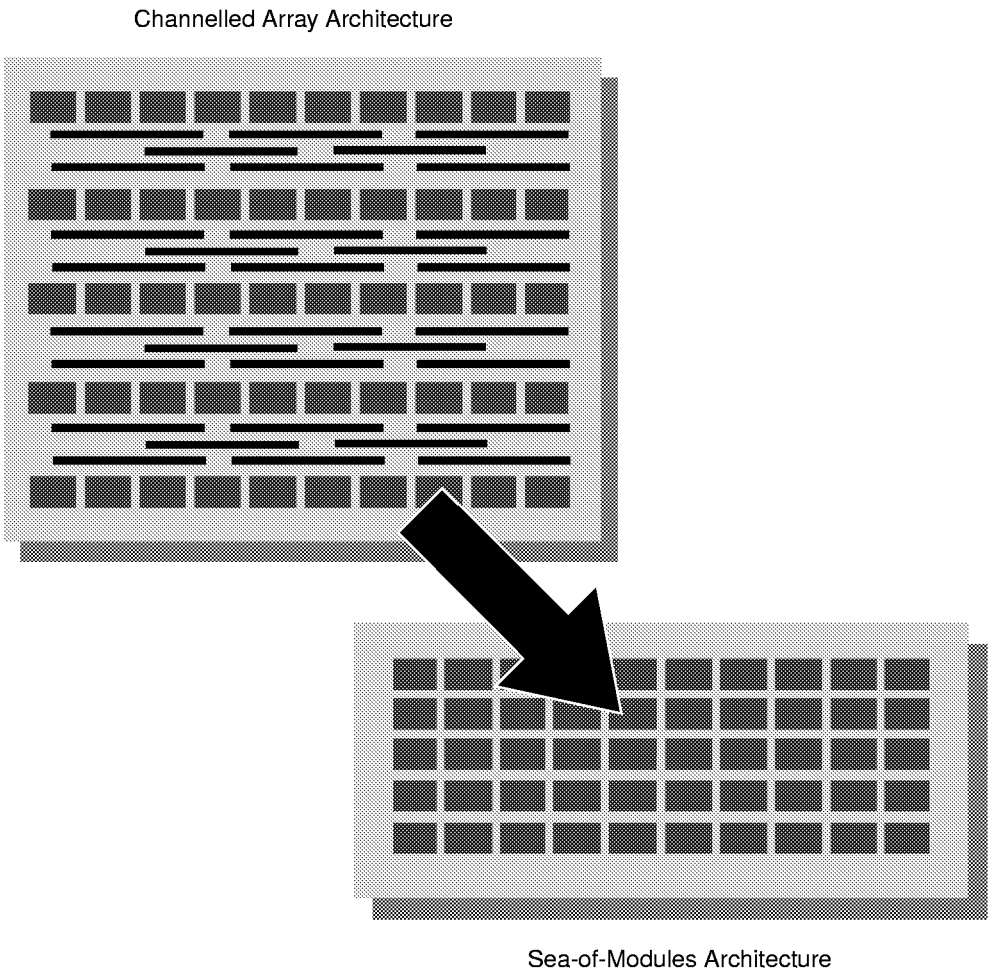


Figure 2 • *Channelled Array and Sea-of-Modules Architectures*

The R-cell (or register cell) contains a flip-flop featuring more control signals than in previous Actel architectures, including asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines). The R-cell (Figure 3) registers feature programmable clock polarity, selectable on a register-by-register basis. This provides the designer with additional flexibility while allowing mapping of synthesized functions into the SX FGPA. The clock source for the R-cell can be chosen from the hard-wired clock or the routed clock.

The C-cell (or combinatorial cell, Figure 4) implements a range of combinatorial functions up to 5-inputs. Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions which can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. This facilitates construction of 9-bit parity-tree functions with 2 ns propagation delays. At the same time, the C-cell structure is extremely synthesis-friendly, simplifying the overall design and reducing synthesis time.

Chip Architecture

The SX Family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

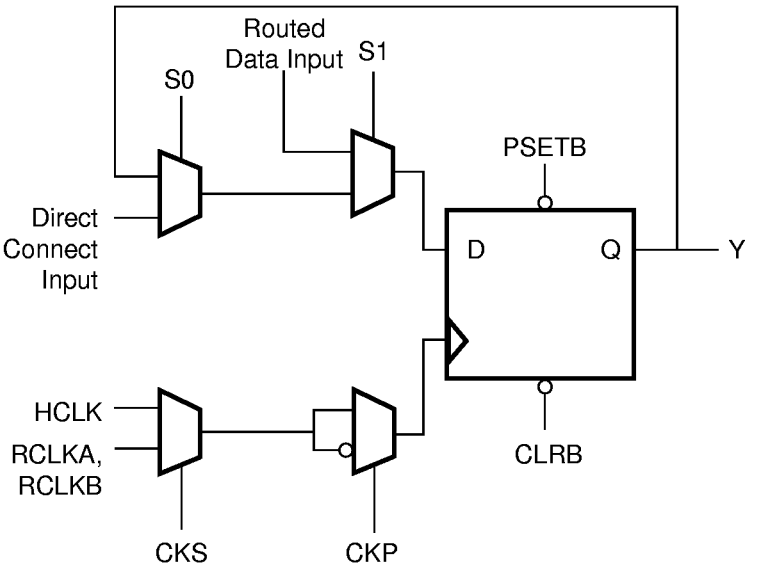


Figure 3 • *R-Cell*

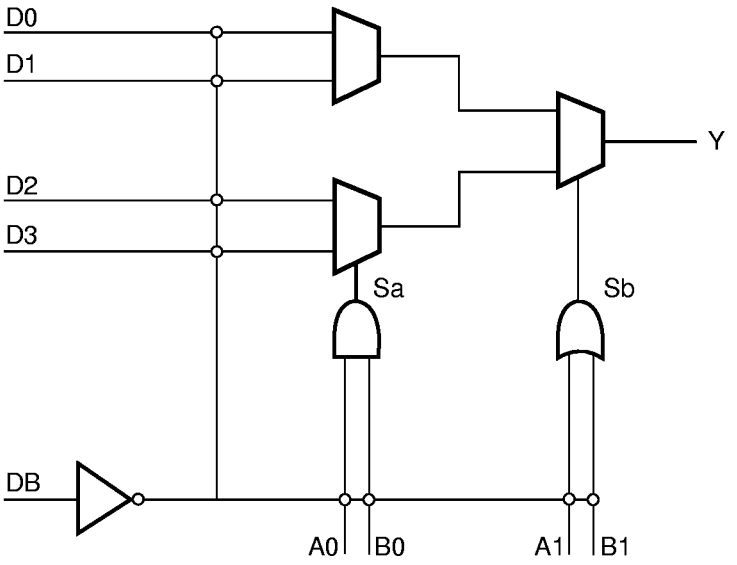


Figure 4 • *C-Cell*

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (see Figure 5). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. SX devices feature significantly more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative new local routing resources called *FastConnect* and *DirectConnect* which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (see Figure 6 and Figure 7). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

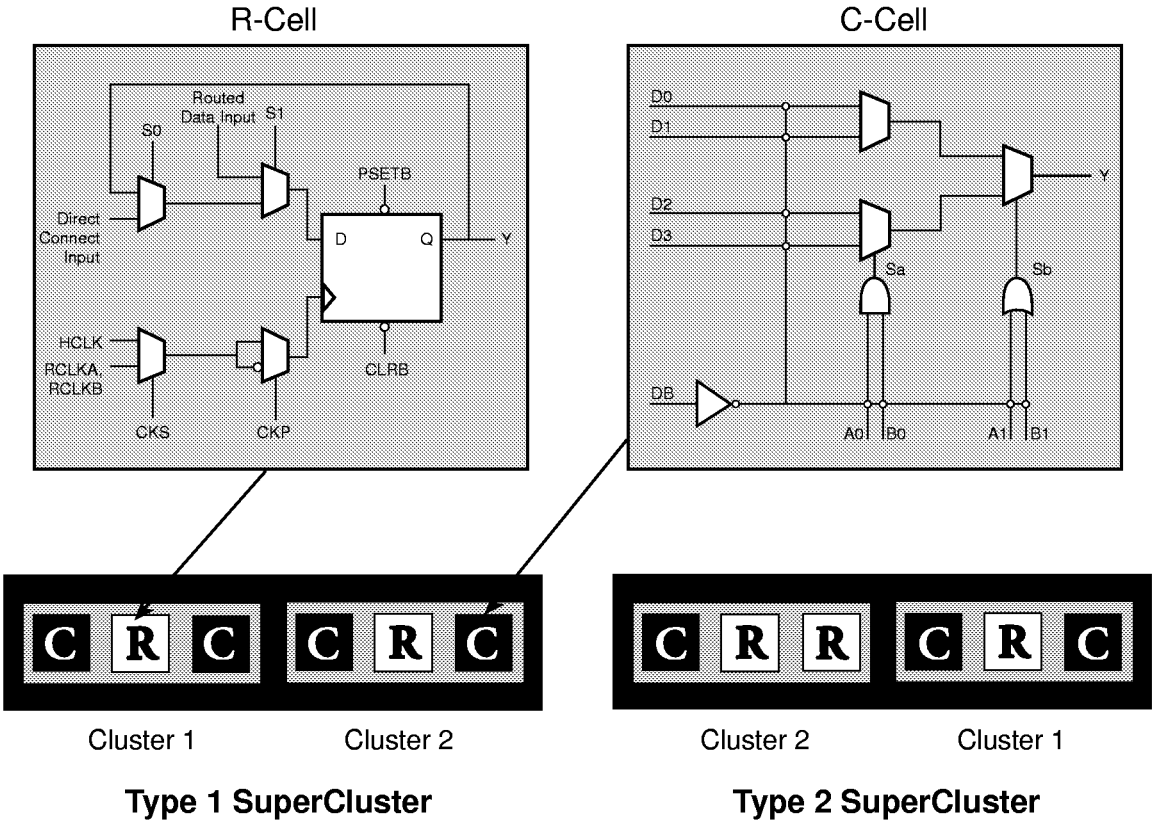


Figure 5 • *Cluster Organization*

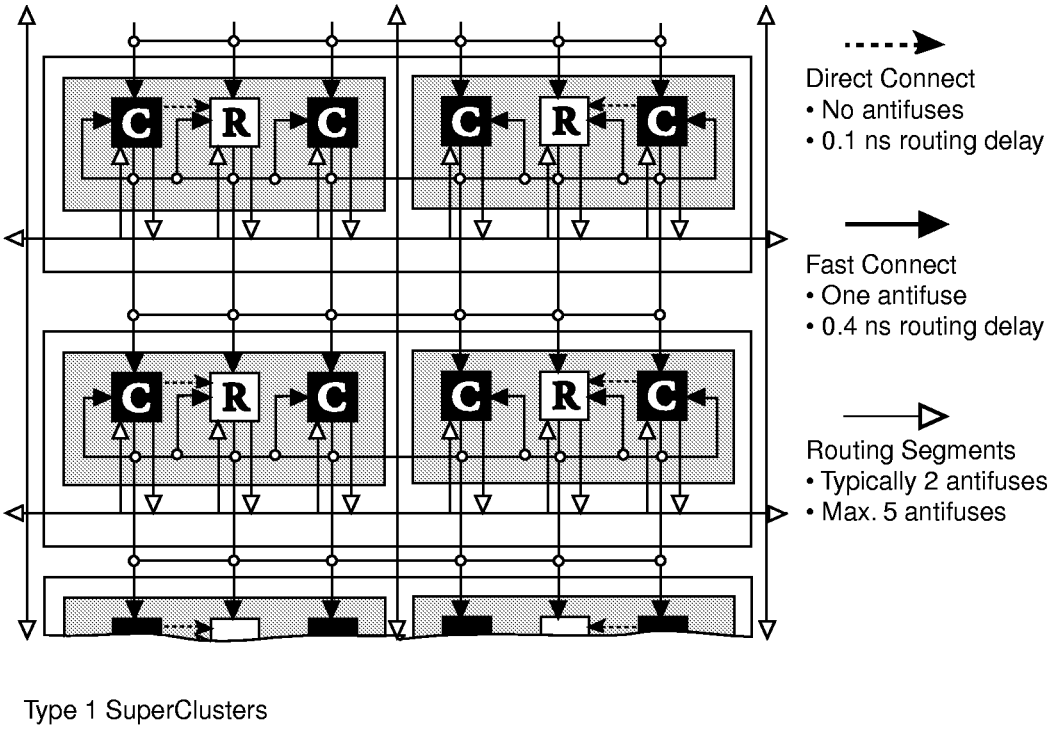


Figure 6 • *DirectConnect and FastConnect for Type 1 SuperClusters*

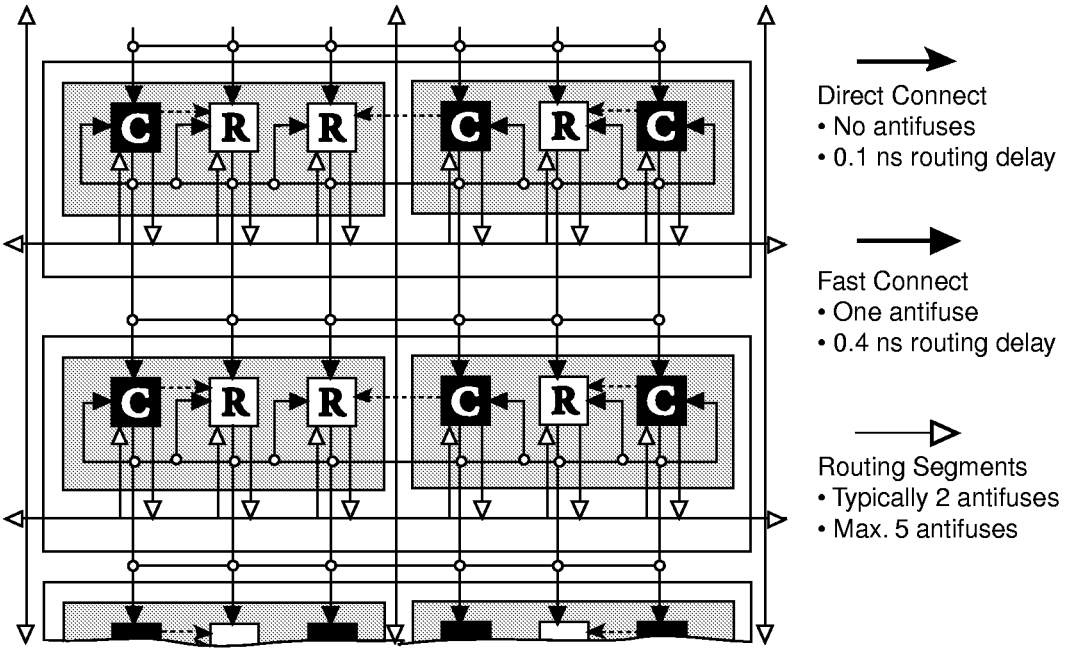


Figure 7 • DirectConnect and FastConnect for Type 2 SuperClusters

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns.

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place and route software to minimize signal propagation delays.

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hard-wired from the HCLK buffer to the clock select MUX in each R-cell. This provides a fast propagation path for the clock signal, enabling the 4.0 ns clock-to-out (pin-to-pin) performance of the SX devices. The hard-wired clock is tuned to provide clock skew as low as 0.25 ns. The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal signal logic within the SX device.

Other Architecture Features

Technology

Actel's SX Family of FPGAs is implemented in high-voltage twin-well CMOS using three layers of metal and 0.35 micron design rules (moving quickly to 0.25 micron). The M2/M3 antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals, and has a programmed ("on" state) resistance of 25 ohms with capacitance of 1.6 fF for low signal impedance.

Performance

The combination of architectural features described above enables SX devices to operate with internal clock frequencies exceeding 300 MHz, enabling very fast execution of even complex logic functions. Thus, the Actel SX Family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs which previously would have required a gate array to meet performance goals can now be integrated into an SX device with dramatic improvements in cost and time-to-market. Using timing-driven place and route tools, designers can achieve highly deterministic device performance.

With SX devices, designers can achieve a higher level of performance without recourse to complicated performance-enhancing design techniques such as the use of redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code.

I/O Modules

Each I/O on an SX device can be configured as an input, an output, a tri-state output, or a bi-directional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 4.0 ns, and external set-up time as low as 0.6 ns. I/O cells including embedded latches and flip-flops require instantiation in HDL code, a complication not required by SX FPGAs. Fast pin-to-pin timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reducing overall design time.

Power Requirements

The SX Family supports 3.3-volt operation and is designed to tolerate 5-volt inputs. Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced due to the small number of antifuses in the path, and because of the low resistance properties of the antifuses. The antifuse architecture does not require active circuitry to hold a charge (as an SRAM or EPROM does), thereby making it the lowest-power architecture on the market.

JTAG

All SX devices feature hard-wired IEEE 1149.1 JTAG Boundary Scan Test circuitry.

Design Tool Support

As with all Actel FPGAs, the new SX Family is fully supported by Actel's Designer Series development tools, which include:

- DirectTime for automated, timing-driven place and route;
- ACTgen for fast development using a wide range of macro functions; and
- ACTmap for logic synthesis.

Designer Series supports industry-leading VHDL- and Verilog-based design tools, including synthesis tools from industry leaders such as Exemplar Logic, Synplicity, and Synopsys.

In addition, the SX Family is supported by Actel's new Silicon Explorer diagnostic and debugging tool kit. Silicon Explorer dramatically reduces verification time from several hours per cycle to a few seconds by enabling real-time, in-circuit debugging. Silicon Explorer includes:

- Probe Pilot, a high-speed signal acquisition and control tool that samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Probe Pilot features 18 probing channels and connects to the user's PC via a standard serial port connection.
- Diagnostic software, which turns the PC into a fully-featured, 100 MHz logic analyzer for easy graphical analysis of waveforms.

Silicon Explorer probes 100 percent of the device circuitry using Probe Pilot's powerful, 18-channel signal acquisition capability. Individual bugs are then isolated and passed to the user interface, providing the user with complete waveform data.

3.3V/5V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CCR}	DC Supply Voltage[2]	–0.3 to +6.0	V
V_{CCA}/V_{CCI}	DC Supply Voltage[2]	–0.3 to +4.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage	–0.5 to +3.6	V
I_{IO}	I/O Source Sink Current[3]	–30 to +5.0	mA
T_{STG}	Storage Temperature	–40 to +125	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diodes will forward-bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range[1]	0 to +70	–40 to +85	°C
3.3V Power Supply Tolerance	±10	±10	%V_{CC}
5V Power Supply Tolerance	±5	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{OH}	(I_{OH} = -20uA) (CMOS)	(V_{CC}-0.1)	V_{CC}	(V_{CC}-0.1)	V_{CC}	V
	(I_{OH} = -8mA) (TTL)	2.4	V_{CC}			
	(I_{OH} = -6mA) (TTL)			2.4	V_{CC}	
V_{OL}	(I_{OL}= 20uA) (CMOS)		0.10			V
	(I_{OL} = 12mA) (TTL)		0.50			
	(I_{OL} = 8mA) (TTL)				0.50	
V_{IL}			0.8		0.8	V
V_{IH}		2.0		2.0		V
t_R, t_F	Input Transition Time t_R, t_F		50		50	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		4.0		4.0	mA
$I_{CC(D)}$	$I_{CC(D)}$ $I_{Dynamic}$ V_{CC} Supply Current		TBD		TBD	mA

Power-Up Sequencing

A54SX08, A54SX16, A54SX32

V_{CCA}	V_{CCR}	V_{CCI}	Power-Up Sequence	Comments
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.

Power-Down Sequencing

A54SX08, A54SX16, A54SX32

V_{CCA}	V_{CCR}	V_{CCI}	Power-Down Sequence	Comments
3.3V	5.0V	3.3V	5.0V First 3.3V Second	No possible damage to device.
			3.3V First 5.0V Second	No possible damage to device.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with three different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a TQFP 176-pin package at commercial temperature and still air is as follows:

$$\text{Absolute Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{jA}\ (\text{°C/W})} = \frac{150\text{°C} - 70\text{°C}}{34\text{°C/W}} = 2.35\text{W}$$

Package Type[1]	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 100 ft/min	θ_{ja} 300 ft/min	θ_{ja} 400 ft/min	Units
Plastic Leaded Chip Carrier (PLCC)	84	11	35	23	17	14	°C/W
Thin Quad Flatpack (TQFP)	176	10	34	22	16	13	°C/W
Very Thin Quad Flatpack (VQFP)	100	10	44	38	32	31	°C/W
Plastic Quad Flatpack (PQFP)	208	6	22	17	15	14	°C/W

Note:

1. *Maximum Power Dissipation in Still Air for 208-pin PQFP package is 3.6 watts, 100-pin VQFP package is 1.8 watts, 176-pin TQFP package is 2.4 watts, 84-pin PLCC package is 2.3 watts.*

Power Dissipation for A54SX16

$$P = [I_{CC}\text{standby} + I_{CC}\text{active}] * V_{CCA} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CCA} - V_{OH}) * M$$

Where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

The power due to standby current is typically a small component of the overall power. Standby power is shown below for commercial, worst case conditions (70°C).

I_{CC}	V_{CC}	Power
4ma	3.6	14.4mW

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totempole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the Equation 1.

$$\text{Power (uW)} = C_{EQ} * V_{CCA}^2 * F \qquad (1)$$

Where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CCA} is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CCA}. Equivalent capacitance is frequency-independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values (pF)

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

Modules (C_{EQM})	7.5
Input Buffers (C_{EQI})	2.0
Output Buffers (C_{EQO})	15.0
Routed Array Clock Buffer Loads (C_{EQCR})	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	0.68
Fixed Capacitance Due to First Routed Array Clock (r_1)	177
Fixed Capacitance Due to Second Routed Array Clock (r_2)	177

$$\text{Power} = V_{CCA}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_CLK}] \quad (2)$$

Where:

- m = Number of logic modules switching at f_m
- n = Number of input buffers switching at f_n
- p = Number of output buffers switching at f_p
- q_1 = Number of clock loads on the first routed array clock
- q_2 = Number of clock loads on the second routed array clock
- r_1 = Fixed capacitance due to first routed array clock
- r_2 = Fixed capacitance due to second routed array clock
- s_1 = Fixed number of clock loads on the dedicated array clock=(528 for 54SX16)
- C_{EQM} = Equivalent capacitance of logic modules in pF
- C_{EQI} = Equivalent capacitance of input buffers in pF
- C_{EQO} = Equivalent capacitance of output buffers in pF
- C_{EQCR} = Equivalent capacitance of routed array clock in pF
- C_{EQCD} = Equivalent capacitance of dedicated array clock in pF
- C_L = Output lead capacitance in pF
- f_m = Average logic module switching rate in MHz
- f_n = Average input buffer switching rate in MHz
- f_p = Average output buffer switching rate in MHz
- f_{q1} = Average first routed array clock rate in MHz
- f_{q2} = Average second routed array clock rate in MHz

Determining Average Switching Frequency

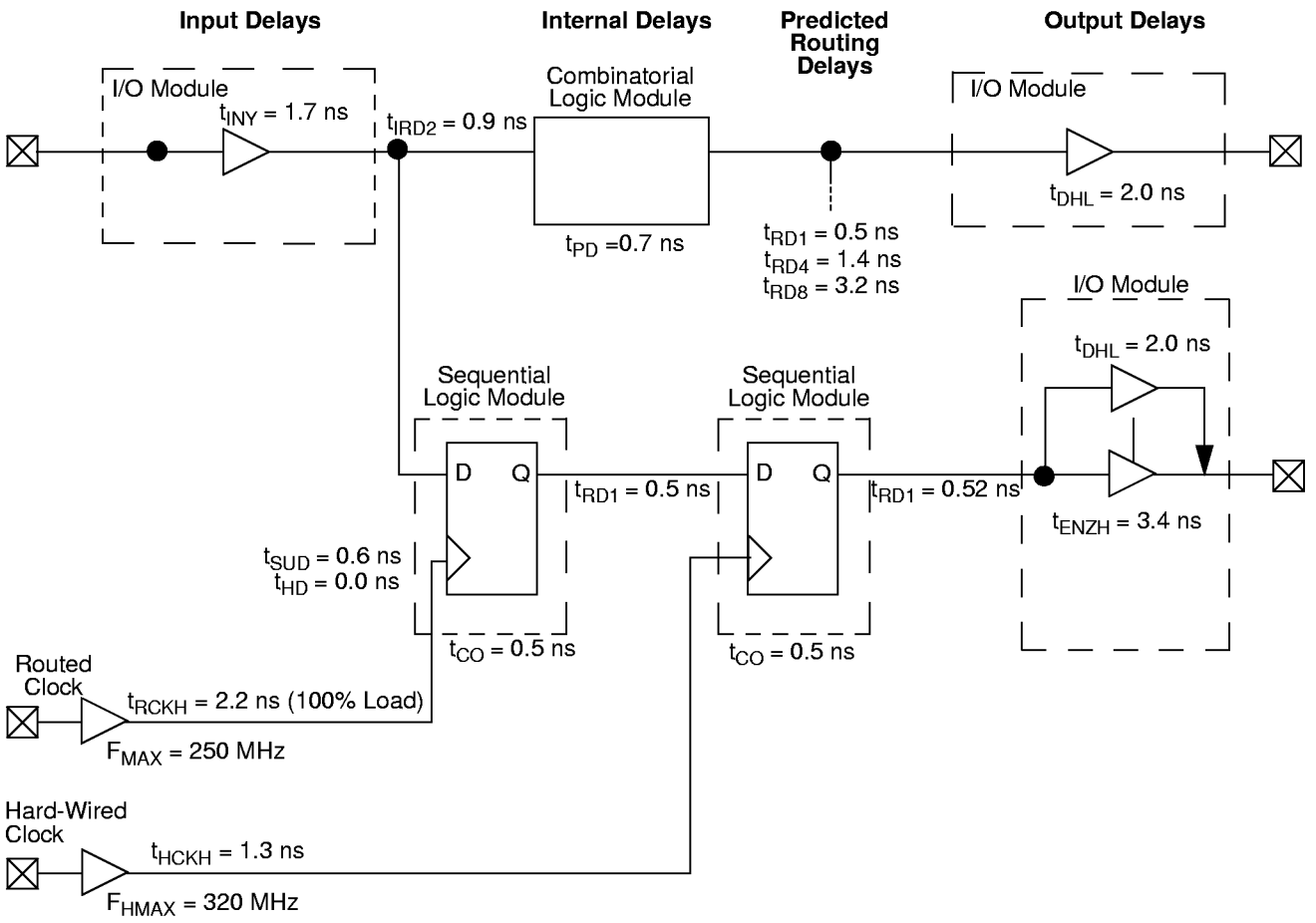
To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

Logic Modules (m)	=	80% of modules
Inputs Switching (n)	=	# inputs/4
Outputs Switching (p)	=	# output/4
First Routed Array Clock Loads (q_1)	=	40% of sequential modules
Second Routed Array Clock Loads (q_2)	=	40% of sequential modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F/2
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	F

Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 3.0V)

	Junction Temperature (T_J)					
V_{CCA}	–40	0	25	70	85	125
3.0	0.78	0.87	0.89	1.00	1.04	1.16
3.3	0.73	0.82	0.83	0.93	0.97	1.08
3.6	0.69	0.77	0.78	0.87	0.92	1.02

54SX Timing Model*



**Values shown for A54SX16-2, worst-case commercial conditions.*

Hard-Wired Clock

External Set-Up = $t_{INY} + t_{IRD1} + t_{SUD} - t_{HCKH}$
= 1.7 + 0.5 + 0.6 – 1.3 = 1.50 ns

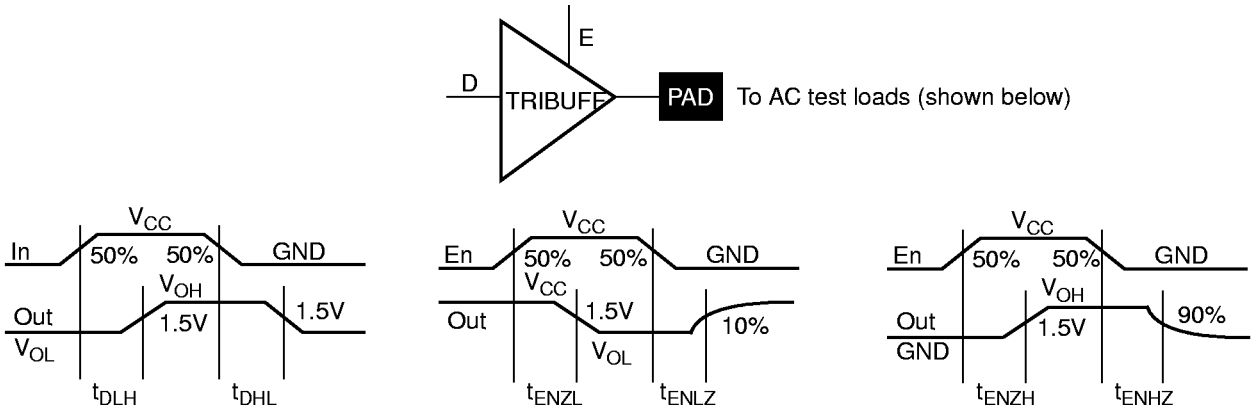
Clock-to-Out (Pin-to-Pin)
= $t_{HCKH} + t_{CO} + t_{RD1} + t_{DHL}$
= 1.3 + 0.5 + 0.5 + 2.1 = 4.4 ns

Routed Clock

External Set-Up = $t_{INY} + t_{IRD1} + t_{SUD} - t_{RCKH}$
= 1.7 + 0.5 + 0.6 – 2.2 = 0.6 ns

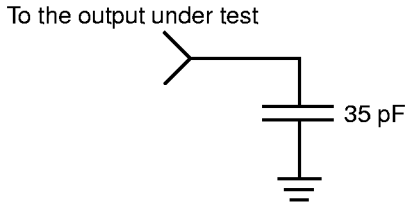
Clock-to-Out (Pin-to-Pin)
= $t_{RCKH} + t_{CO} + t_{RD1} + t_{DHL}$
= 2.2 + 0.5 + 0.5 + 2.1 = 5.3 ns

Output Buffer Delays

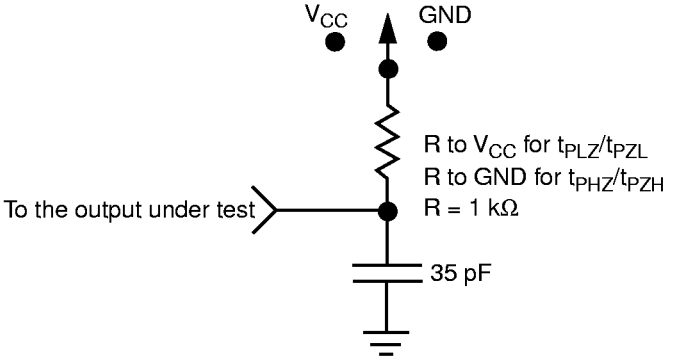


AC Test Loads

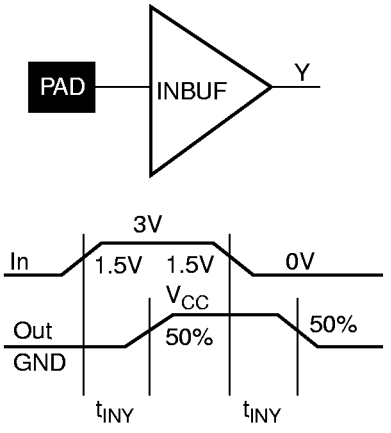
Load 1
(Used to measure propagation delay)



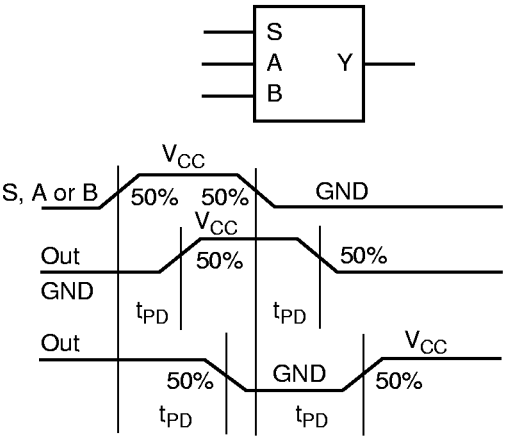
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

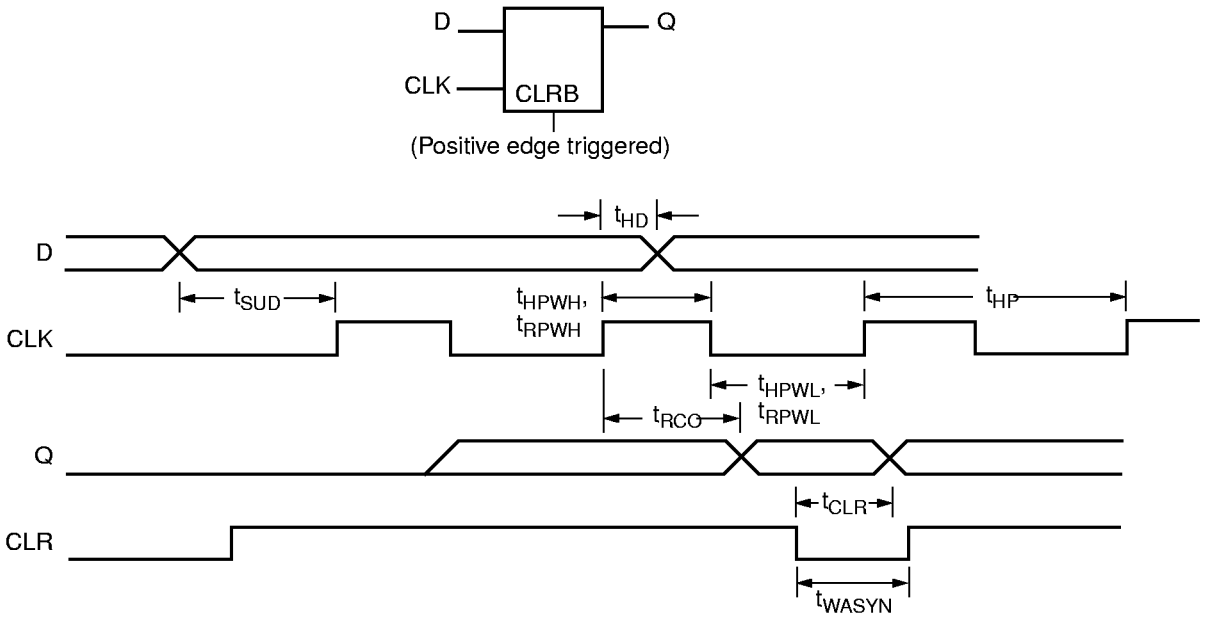


C-Cell Delays



Sequential Module Timing Characteristics

Flip-Flops



Timing Characteristics

Timing characteristics for 54SX devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all 54SX family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the DirectTime Analyzer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 12.6 ns delay. This additional delay is represented statistically in higher fanout (FO=24) routing delays in the data sheet specifications section.

Timing Derating

54SX devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

A54SX16 Timing Characteristics

(Worst-Case Commercial Conditions, V_{CCR}= 4.75 V, V_{CCA},V_{CCI} = 3.0 V, T_J = 70°C)

C-Cell Propagation Delays[1]		**'–2' Speed**		**'–1' Speed**		**'Std' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		0.7		0.8		0.9	ns
Predicted Routing Delays[2]								
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.4		0.5		0.6	ns
t_{RD1}	FO=1 Routing Delay		0.5		0.6		0.7	ns
t_{RD2}	FO=2 Routing Delay		0.9		1.0		1.2	ns
t_{RD3}	FO=3 Routing Delay		1.3		1.5		1.7	ns
t_{RD4}	FO=4 Routing Delay		1.4		1.9		2.2	ns
t_{RD8}	FO=8 Routing Delay		3.2		3.7		4.3	ns
t_{RD12}	FO=12 Routing Delay		3.6		4.8		5.7	ns
t_{RD18}	FO=18 Routing Delay		7.1		8.1		9.5	ns
t_{RD24}	FO=24 Routing Delay		9.5		10.7		12.6	ns
R-Cell Timing								
t_{RCO}	Sequential Clock-to-Q		0.5		0.5		0.7	ns
t_{CLR}	Asynchronous Clear-to-Q		0.5		0.5		0.7	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.6		0.7		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.9		2.1		2.5		ns

Notes:

1. *For dual-module macros, use t_{PD} + t_{RD1} + t_{PDn} , t_{RCO} + t_{RD1} + t_{PDn} or t_{PD1} + t_{RD1} + t_{SUD} , whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

I/O Module Input Propagation Delays		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Input Data Pad-to-Y HIGH		1.7		1.9		2.2	ns
t_{INYL}	Input Data Pad-to-Y LOW		1.7		1.9		2.2	ns
Predicted Input Routing Delays[1]								
t_{IRD1}	FO=1 Routing Delay		0.5		0.6		0.7	ns
t_{IRD2}	FO=2 Routing Delay		0.9		1.0		1.2	ns
t_{IRD3}	FO=3 Routing Delay		1.3		1.5		1.7	ns
t_{IRD4}	FO=4 Routing Delay		1.4		1.9		2.2	ns
t_{IRD8}	FO=8 Routing Delay		3.2		3.7		4.3	ns
t_{IRD12}	FO=12 Routing Delay		3.6		4.8		5.7	ns
t_{IRD18}	FO=18 Routing Delay		7.1		8.1		9.5	ns
t_{IRD24}	FO=24 Routing Delay		9.5		10.7		12.6	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

A54SX16 Timing Charateristics(continued)

(Worst-Case Commercial Conditions)

I/O Module – TTL Output Timing[1]		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DLH}	Data-to-Pad LOW to HIGH		2.1		2.4		2.8	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.1		2.4		2.8	ns
t_{ENZL}	Enable-to-Pad, Z to L		1.8		2.0		2.4	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.1		2.4		2.8	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.4		3.9		4.5	ns
t_{ENHZ}	Enable-to-Pad, H to Z		1.7		1.9		2.2	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04		0.05	ns/pF
d_{THL}	Delta HIGH to LOW		0.03		0.04		0.07	ns/pF

Note:

1. Delays based on 35pF loading.

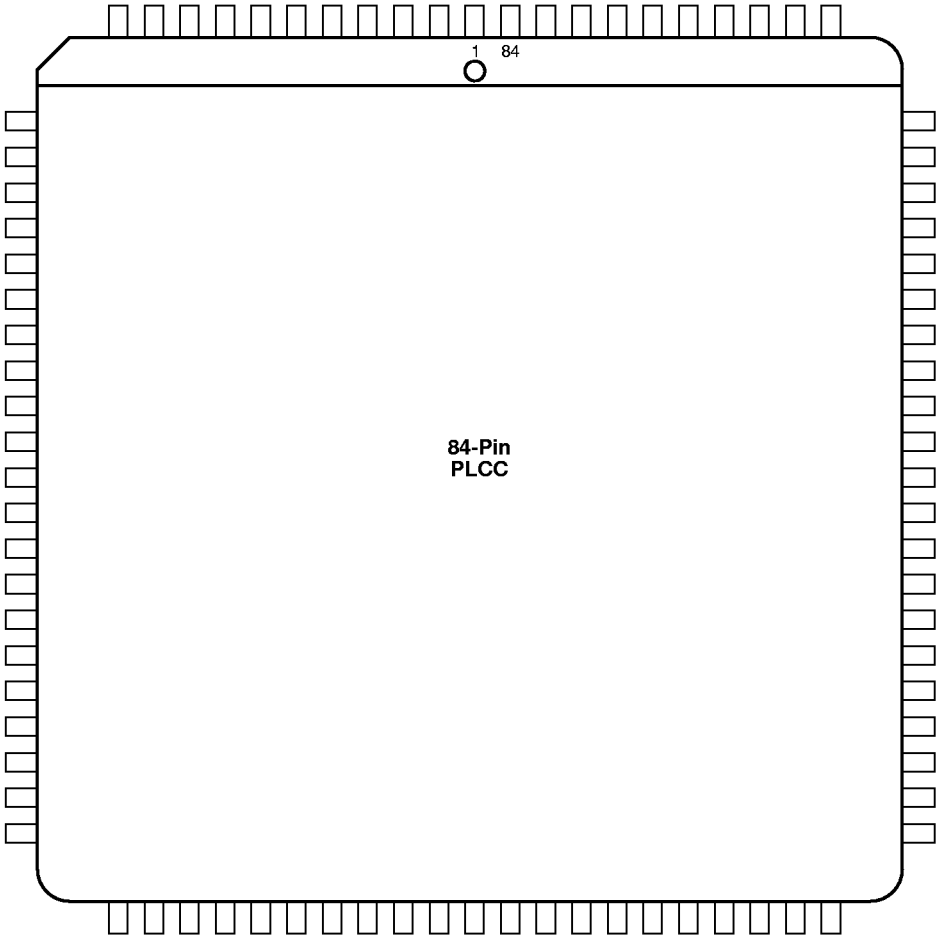
A54SX16 Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

Dedicated (Hard-Wired) Array Clock Network		'–2' Speed		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		1.3		1.5		1.7	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		1.4		1.6		1.9	ns
t_{HPWH}	Minimum Pulse Width HIGH	1.6		1.8		2.1		ns
t_{HPWL}	Minimum Pulse Width LOW	1.6		1.8		2.1		ns
t_{HCKSW}	Maximum Skew		0.2		0.3		0.3	ns
t_{HP}	Minimum Period	3.1		3.6		4.2		ns
f_{HMAX}	Maximum Frequency		320		280		240	MHz
Routed Array Clock Networks								
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		1.8		2.1		2.5	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		2.0		2.3		2.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		2.1		2.5		2.8	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		2.2		2.5		3.0	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		2.1		2.4		2.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		2.2		2.5		3.0	ns
t_{RPWH}	Min. Pulse Width HIGH	2.4		2.7		3.2		ns
t_{RPWL}	Min. Pulse Width LOW	2.4		2.7		3.2		ns
t_{RCKSW}	Maximum Skew (Light Load)		0.5		0.5		0.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		0.6		0.7		0.8	ns
t_{RCKSW}	Maximum Skew (100% Load)		0.6		0.7		0.8	ns

Package Pin Assignments

84-Pin PLCC (Top View)



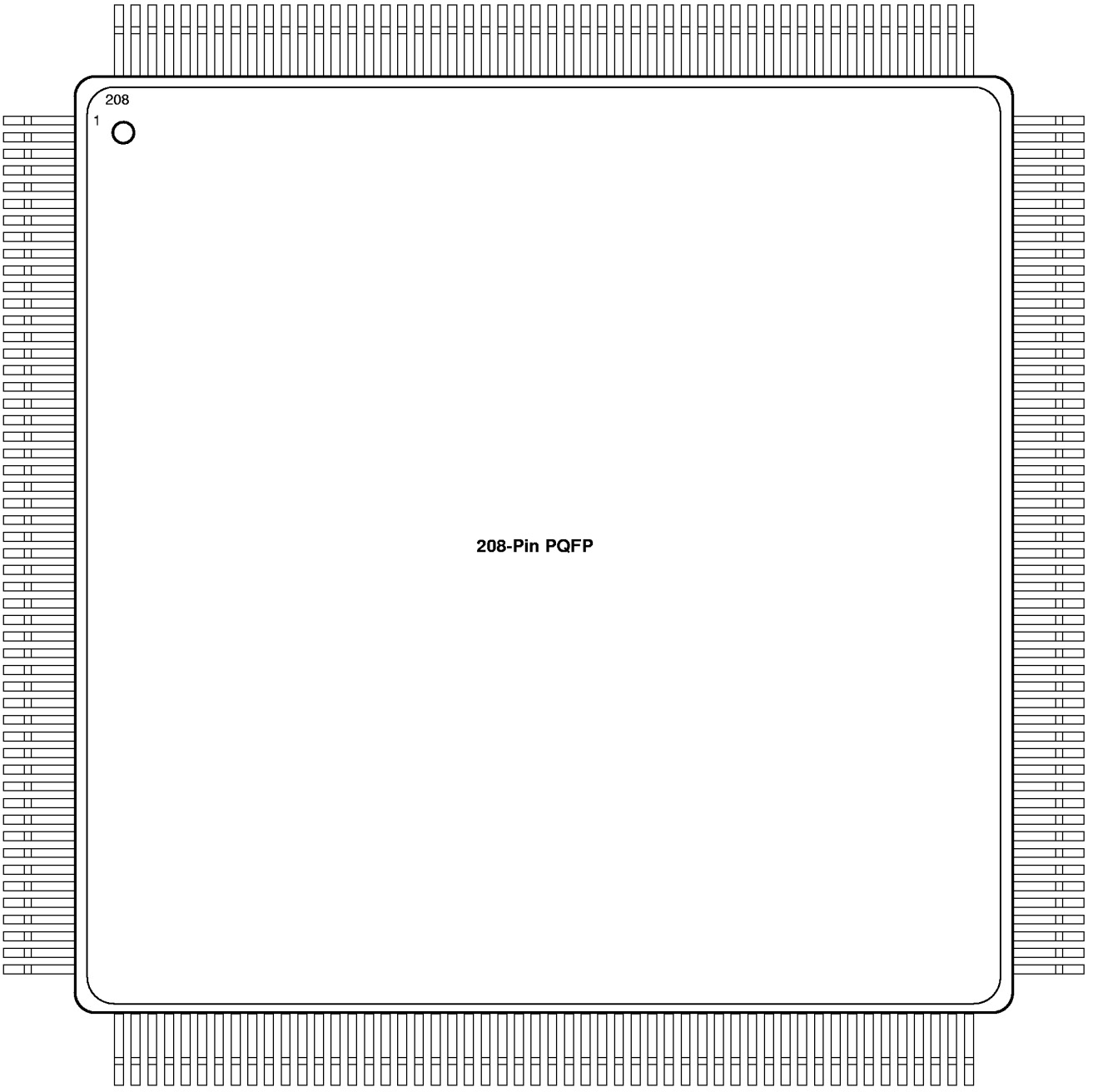
84-Pin PLCC

PKG PIN #	FUNCTION
1	V_{CCR}
2	GND
3	V_{CCA}
4	PRA, I/O
5	I/O
6	V_{CCI}
7	I/O
8	I/O
9	I/O
10	I/O
11	TCK, I/O
12	TDI, I/O
13	I/O
14	I/O
15	I/O
16	TMS
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	GND
28	V_{CCI}
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	PRB, I/O
41	V_{CCA}
42	GND

PKG PIN #	FUNCTION
43	V_{CCR}
44	I/O
45	HCLK
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	TDO, I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	V_{CCA}
60	V_{CCI}
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	V_{CCA}
69	GND
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	CLKA
84	CLKB

Package Pin Assignments **(continued)**

208-Pin PQFP



208-Pin PQFP

PIN #	FNCTN
1	GND
2	TDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	TMS
12	V_{CCI}
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	V_{CCR}
26	GND
27	V_{CCA}
28	GND
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	V_{CCI}
41	V_{CCA}
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	GND

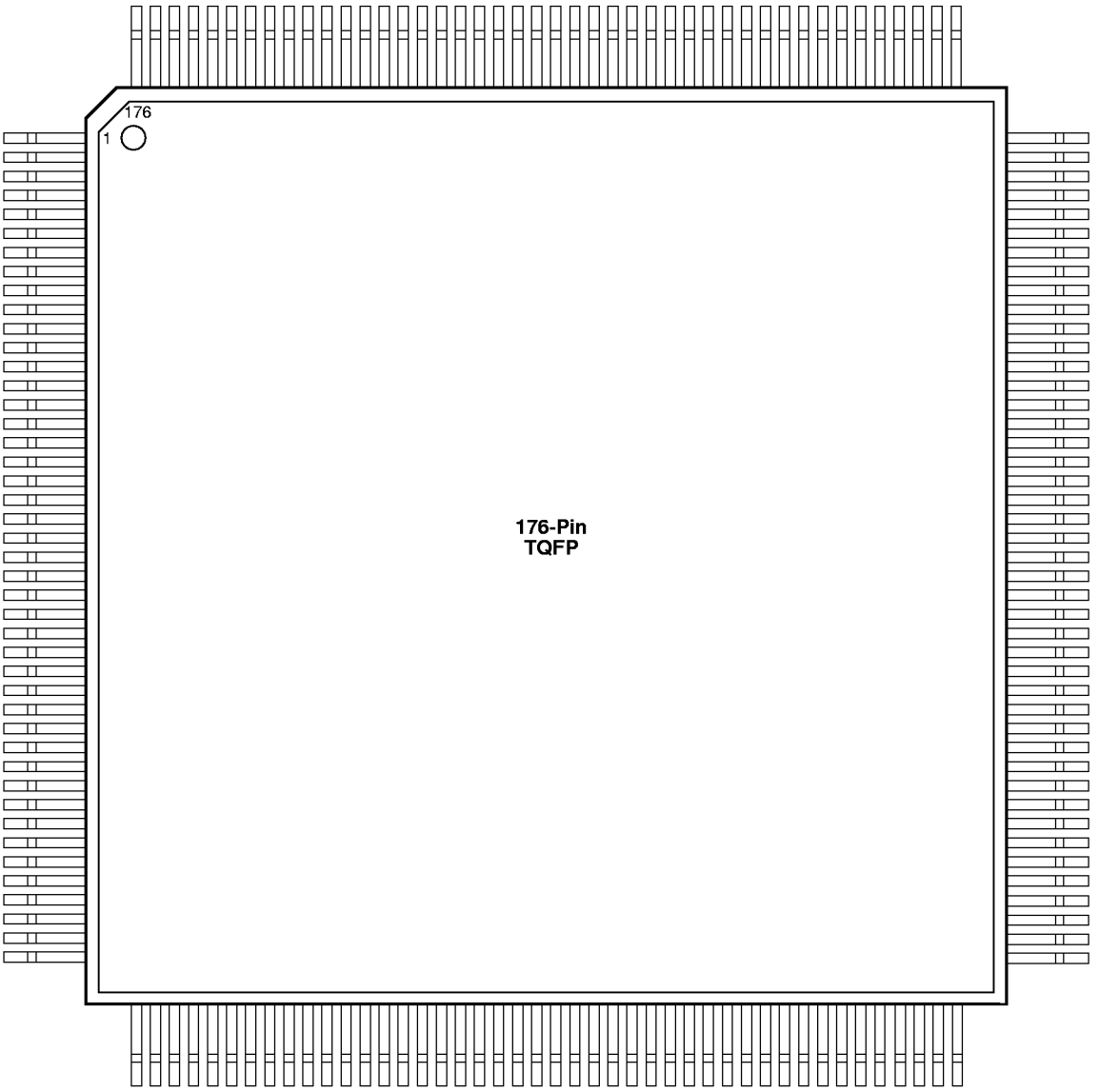
PIN #	FNCTN
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	I/O
60	V_{CCI}
61	I/O
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	PRB, I/O
77	GND
78	V_{CCA}
79	GND
80	V_{CCR}
81	I/O
82	HCLK
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	V_{CCI}
99	I/O
100	I/O
101	I/O
102	I/O
103	TDO, I/O
104	I/O

PIN #	FNCTN
105	GND
106	I/O
107	I/O
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	V_{CCA}
115	V_{CCI}
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	GND
130	V_{CCA}
131	GND
132	V_{CCR}
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	I/O
141	I/O
142	I/O
143	I/O
144	I/O
145	V_{CCA}
146	GND
147	I/O
148	V_{CCI}
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O

PIN #	FNCTN
157	GND
158	I/O
159	I/O
160	I/O
161	I/O
162	I/O
163	I/O
164	V_{CCI}
165	I/O
166	I/O
167	I/O
168	I/O
169	I/O
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	I/O
177	I/O
178	I/O
179	I/O
180	CLKA
181	CLKB
182	V_{CCR}
183	GND
184	V_{CCA}
185	GND
186	PRA, I/O
187	I/O
188	I/O
189	I/O
190	I/O
191	I/O
192	I/O
193	I/O
194	I/O
195	I/O
196	I/O
197	I/O
198	I/O
199	I/O
200	I/O
201	V_{CCI}
202	I/O
203	I/O
204	I/O
205	I/O
206	I/O
207	I/O
208	TCK, I/O

Package Pin Assignments (continued)

176-Pin TQFP (Top View)



176-Pin TQFP

PIN #	FNCTN
1	GND
2	TDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	TMS
11	V_{CCI}
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND
22	V_{CCA}
23	GND
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	V_{CCI}
33	V_{CCA}
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	GND

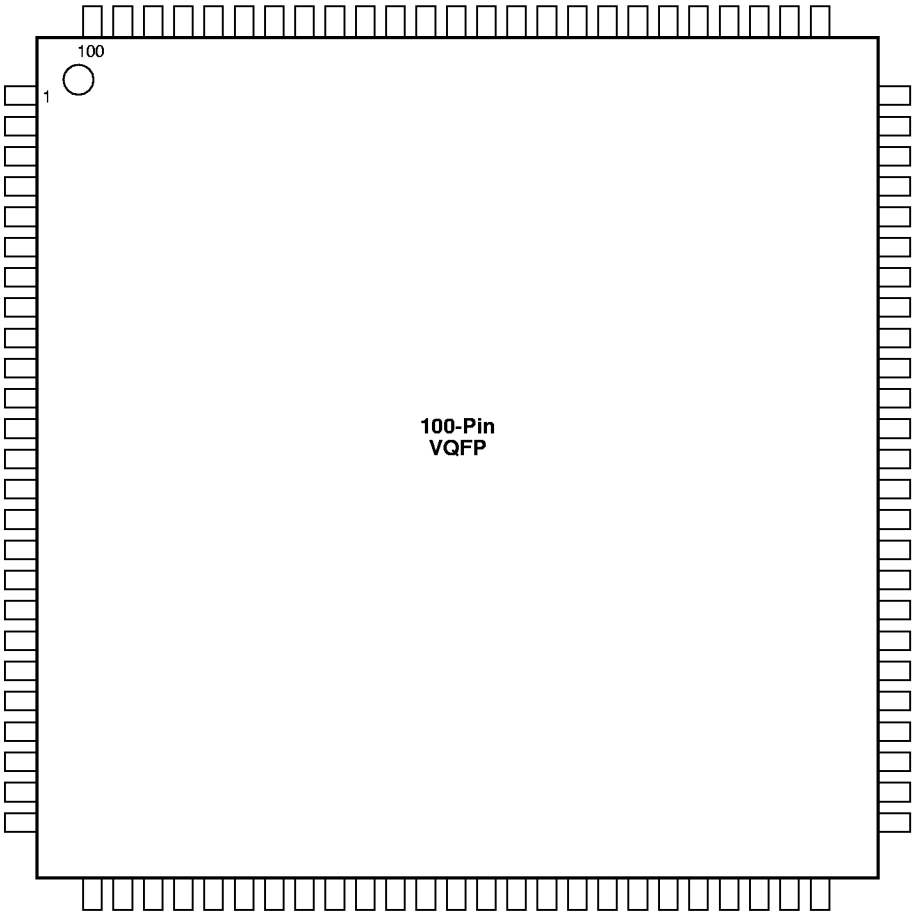
PIN #	FNCTN
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	V_{CCI}
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	PRB, I/O
65	GND
66	V_{CCA}
67	V_{CCR}
68	I/O
69	HCLK
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	V_{CCI}
83	I/O
84	I/O
85	I/O
86	I/O
87	TDO, I/O
88	I/O

PIN #	FNCTN
89	GND
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	V_{CCA}
99	V_{CCI}
100	I/O
101	I/O
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	GND
109	V_{CCA}
110	GND
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	I/O
120	I/O
121	I/O
122	V_{CCA}
123	GND
124	V_{CCI}
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O

PIN #	FNCTN
133	GND
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	I/O
140	V_{CCI}
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	CLKA
153	CLKB
154	V_{CCR}
155	GND
156	V_{CCA}
157	PRA, I/O
158	I/O
159	I/O
160	I/O
161	I/O
162	I/O
163	I/O
164	I/O
165	I/O
166	I/O
167	I/O
168	I/O
169	V_{CCI}
170	I/O
171	I/O
172	I/O
173	I/O
174	I/O
175	I/O
176	TCK, I/O

Package Pin Assignments (continued)

100-Pin VQFP (Top View)



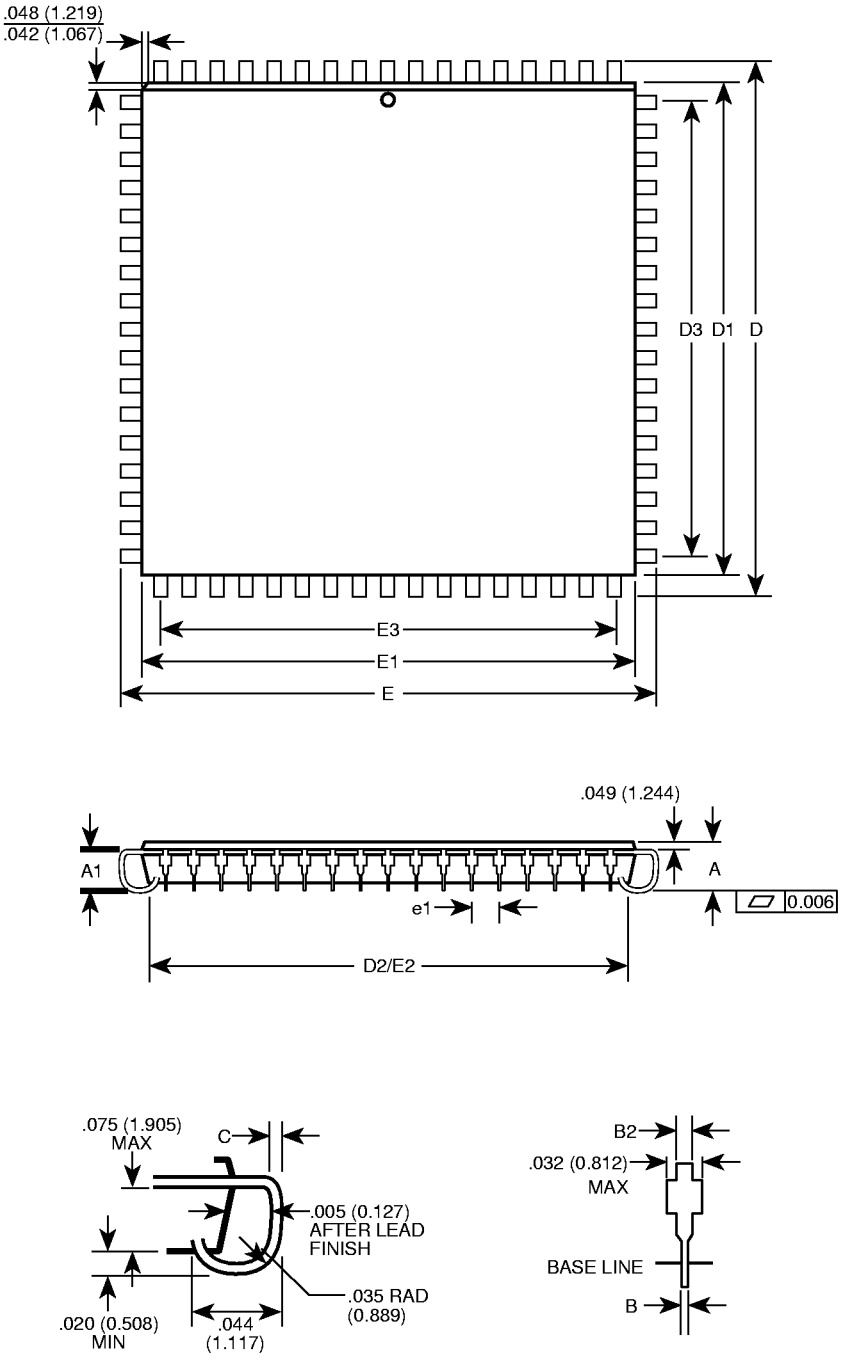
100-VQFP

PKG PIN #	FUNCTION
1	GND
2	TDI, I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	TMS
8	V_{CCI}
9	GND
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	V_{CCI}
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	PRB, I/O
35	V_{CCA}
36	GND
37	V_{CCR}
38	I/O
39	HCLK
40	I/O
41	I/O
42	I/O
43	I/O
44	V_{CCI}
45	I/O
46	I/O
47	I/O
48	I/O
49	TDO, I/O
50	I/O

PKG PIN #	FUNCTION
51	GND
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	V_{CCA}
58	V_{CCI}
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	V_{CCA}
68	GND
69	GND
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	V_{CCI}
83	I/O
84	I/O
85	I/O
86	I/O
87	CLKA
88	CLKB
89	V_{CCR}
90	V_{CCA}
91	GND
92	PRA, I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	TCK, I/O

Package Mechanical Drawings

Plastic Leaded Chip Carrier (PLCC)



Plastic Leaded Chip Carrier Packages (PLCC)

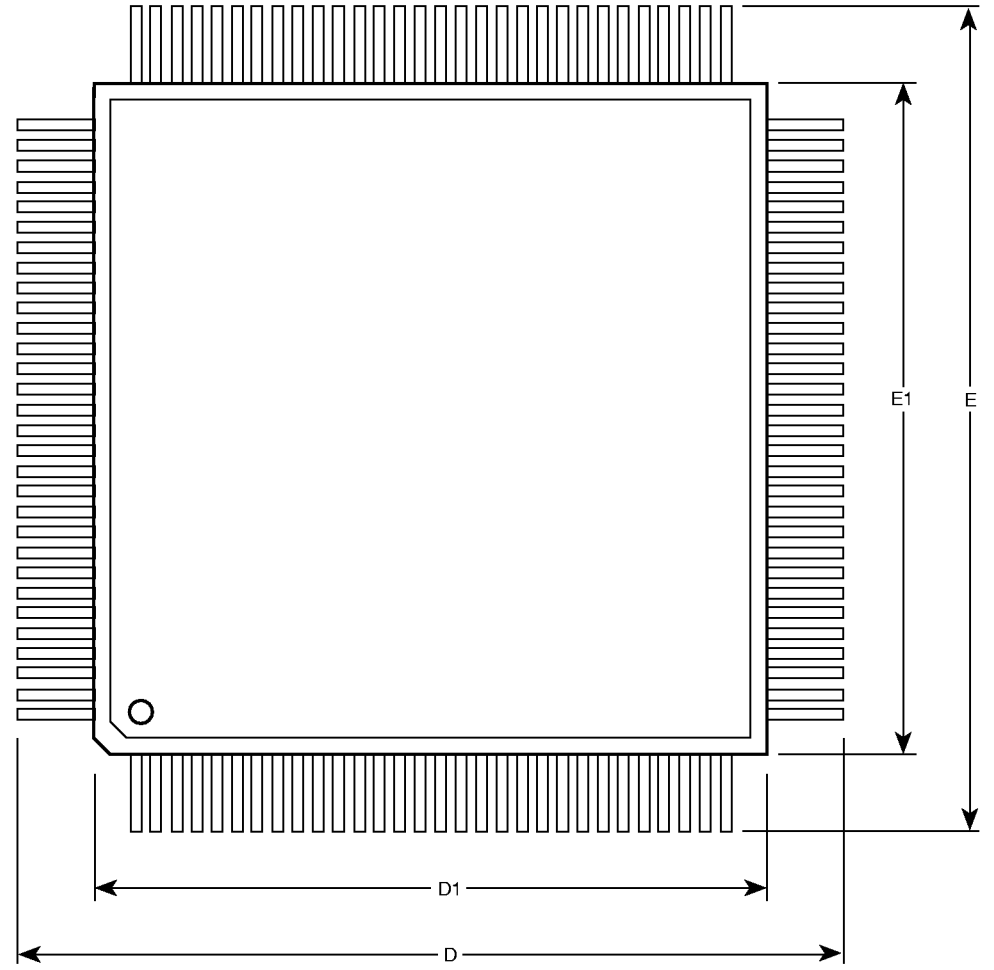
JEDEC Equivalent	PLCC84 MS007 AE VAR	
Dimension	**Min.**	**Max.**
A	0.155	0.175
A1	0.090	0.130
B	0.013	0.027
B2	0.026	0.032
C	0.005	0.011
D/E	1.170	1.210
D1/E1	1.140	1.160
D2/E2	1.090	1.130
D3/E3	1.00 nominal	
e1	0.050 BSC	

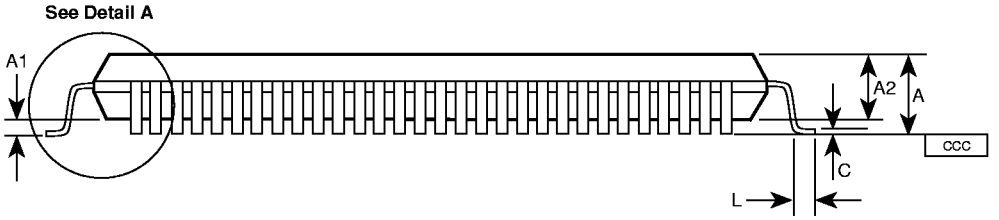
Notes:

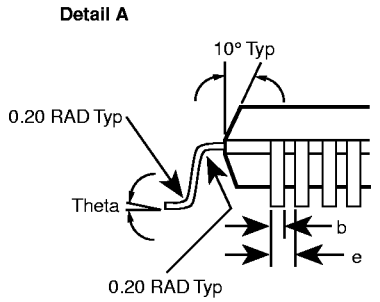
1. *All dimensions are in inches.*
2. *BSC—Basic Spacing between Centers.*

Package Mechanical Drawings (continued)

Plastic Quad Flat Pack (PQFP, TQFP, VQFP)







Plastic Quad Flat Packages (PQFP)

JEDEC Equivalent	PQFP208 M0-143	
Dimension	**Min.**	**Max.**
A		4.10
A1	0.25	
A2	3.20	3.60
b	0.17	0.27
c	0.09	0.20
D	30.60 BSC	
D1	28.00 BSC	
E	30.60 BSC	
E1	28.00 BSC	
e	0.50 BSC	
L	0.50	0.75
ccc		0.08
Theta	0	7 deg

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

Thin Quad Flat Packs (TQFP and VQFP)

JEDEC Equivalent	TQFP176 M0-136		VQFP100 M0-136	
Dimension	**Min.**	**Max.**	**Min.**	**Max.**
A		1.60		1.20
A1	0.05	0.15	0.05	0.15
A2	1.35	1.45	0.95	1.05
b	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20
D/E	26.00 BSC		16.00 BSC	
D1/E1	24.00 BSC		14.00 BSC	
e	0.50 BSC		0.50 BSC	
L	0.45	0.75	0.45	0.75
ccc		0.08		0.08
Theta	0	7 deg	0	7 deg

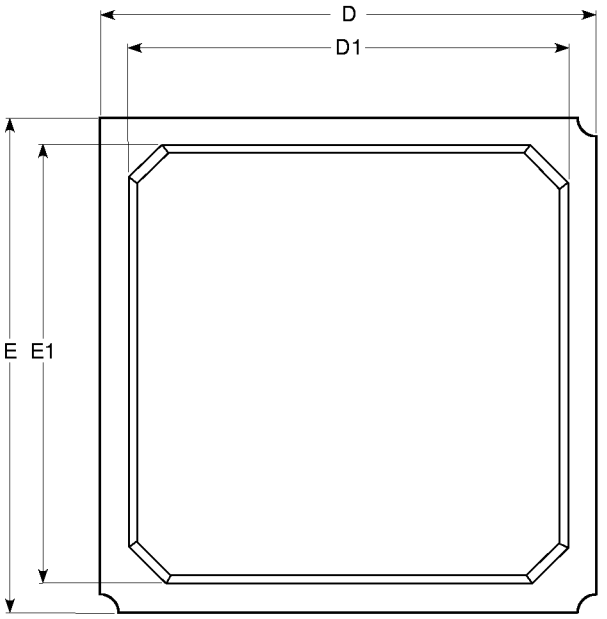
Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*

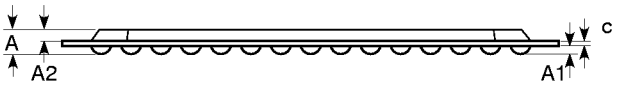
Package Mechanical Drawings (continued)

Ball Grid Array (BGA)

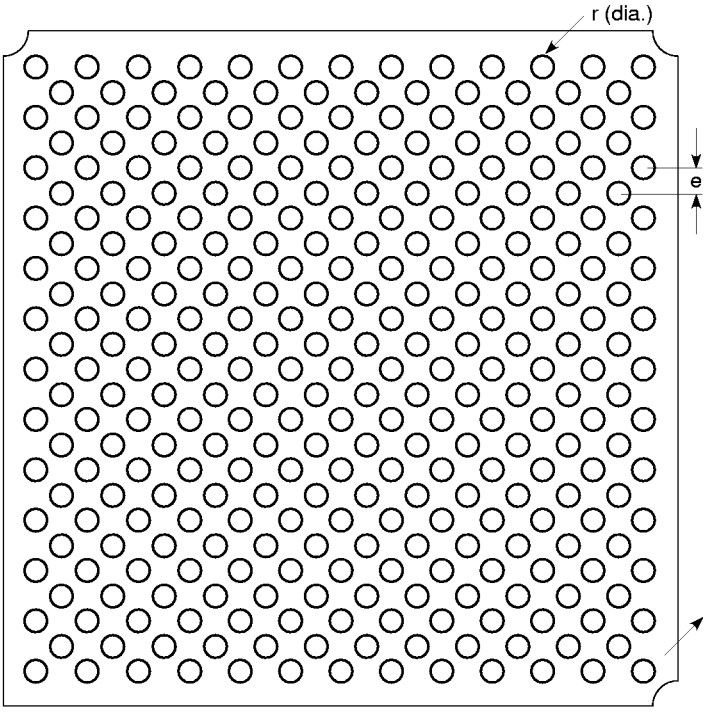
Top View



Side View



Bottom View
313 BGA



Plastic Ball Grid Array (PBGA)

JEDEC Equivalent	BGA 313 MO-151	
Dimension	**Min.**	**Max.**
A2	1.12	1.22
A1	0.50	0.70
c	0.56 REF.	
A	2.12	2.52
D/E	34.80	35.20
D1/E1	30.00	30.70
e	0.50 BSC	
r (diameter)	0.60	0.90

Notes:

1. *All dimensions are in millimeters.*
2. *BSC—Basic Spacing between Centers.*